Application Bulletin AB-16

Designing the Input Filter for a Pentium II Processor Converter

Summary

The input filter of a Pentium II converter reduces the ripple current and voltage seen by the power source, and can be used to reduce the rate of change of current as well. The parameters determining the sizing of this filter are the ripple current rating of the input capacitors and the dI/dt required by the input line.

Why is an Input Filter Necessary?

A buck converter draws current in approximately rectangular pulses (see Figure 1). The resultant voltage pulses on the source line may be enough to upset other devices. The current pulses are also a prime source of EMI (Electromagnetic Interference), since the current is large and the edge transitions are fast. For both of these reasons, the current drawn by the buck converter should be filtered.

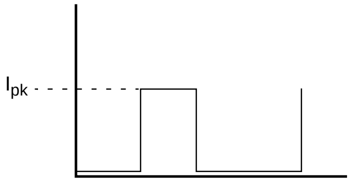

Figure 1. A Buck Converter Draws Rectangular Pulses of Current from the Power Source

Filtering the current drawn by a buck can be accomplished by adding low-ESR capacitors to the input of the converter, see Figure 2. [ESR = Equivalent Series Resistance.] The voltage seen on the line is then I_{pk} x ESR. However, there can still be noise problems: When a fast load step occurs on the output of the converter, it also shows up as a transient on the input of the converter. The energy cannot come indefinitely from the input caps: the input current must increase. For Pentium II converters, Intel specifies that the maximum rate of change of current, dI/dt, should not exceed 0.1A/µsec. Adding an input inductor to the filter can control the dI/dt.

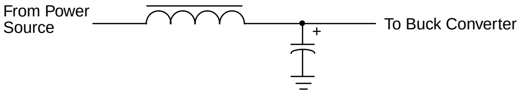

Figure 2. Typical Input Filter

Selecting the Input Capacitance

For the values of inductance and capacitance typically necessary for a Pentium II buck converter input filter, the impedance of the inductance at the switching frequency is very high compared with the impedance of the capacitance. Therefore, essentially all of the AC current comes from the capacitors.

Since capacitors have ESR, AC current passing through them gives rise to self-heating ($P = I_{RMS}^2$ x ESR). This sets a limit on how much AC current can be passed through a given capacitor without overheating it, dependent on its ESR and the package size. Ultimately, this self-heating causes capacitors to fail. *Note that only capacitors that have ESR rated at 100kHz should be used for the input filter!* It is typical to use capacitors that have a rated life of at least 2000 hours; better built converters will use 5000 hour parts.

Rather than specifying thermal resistance in °C/W for each capacitor package, manufacturers typically specify a maximum RMS ripple current. This ripple current rating is a function of temperature, and the temperature used for the assessment should be the average ambient temperature the capacitor will see over its operating life.

As a typical example, consider Sanyo 10MV1200GX capacitors. These have a ripple current rating of 1.25A at 105°C from 10kHz to 200kHz, and a rated life of 10,000 hours. Using data available from the manufacturer, these parts allow an increase of ripple current for temperatures < 65°C by a factor of 1.6, so that their actual-use ripple rating is 2.0Arms.

We can now calculate the actual RMS ripple current. First, remember that the current shown in Figure 1 is the total drawn by the converter, which includes both AC and DC—but the capacitors source only AC. The current is I_{pk} during the on-time of the buck transistor, and zero during the off-time. So we need to find the DC average: $I_{avg} = I_{pk}$ x dc, where dc = duty cycle. Subtracting this off leaves the AC component:

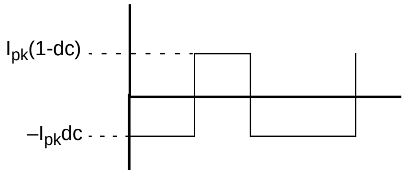

Figure 3. AC Component of Buck Converter Input Current

During the on-time, the current is $I_{pk} - I_{avg} = I_{pk}$ x (1 - dc), and during the off-time the current is $-I_{avg} = -I_{pk}$ x dc. Note that positive current is defined as coming out of the capacitor.

To find the RMS (root-mean-*square*) we now square this waveform:

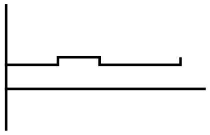

Figure 4. AC Current of Figure 3 Squared

During the on-time, the current squared is $[I_{pk} \text{ x } (1 - dc)]^2$, and during the off-time it is $[-I_{pk} \text{ x } dc]^2$. Adding these together for their respective times, time = dc for the on-time and (1 - dc) for the off-time, (the *mean* part) gives after algebra

$$I_{pk}^2(1-dc)^2dc + I_{pk}^2dc^2(1-dc) = I_{pk}^2(dc - dc^2)$$

Finally, taking the square root (the *root* part) gives the RMS current as:

$$I_{RMS} = I_{pk}\sqrt{(DC - DC^2)}$$

Example: A 400MHz Deschutes Pentium II power supply, supplying 12.6A maximum at 2.0V with an input voltage of 5V.

We estimate average processor current as 12.6A x 75% = 9.45A. Duty cycle is dc = 2.0V / 5V = 0.4. I_{RMS} = 9.45A x $(0.4 - 0.4^2)^{1/2}$ = 4.6A. Using Sanyo 10MV1200GX capacitors with a rating of 2.0A per, the supply should use three caps.

It should be noted that this calculation shows the *minimum* number of capacitors to be used; using more may improve their life expectancy.

Selecting the Input Inductor

The input inductance may be determined by the dI/dt requirement and the input capacitors that have been selected. Basically, a load step on the output must translate into a load step on the input; the relative impedances of the inductor and capacitor determine how fast the current in the inductor rises. The analytical expression for the dI/dt is very complex, but fortunately it isn't needed. We can reason as follows.

The maximum dI/dt occurs when the maximum voltage is applied across the inductor. Since one end of the inductor is presumed fixed at the DC input voltage, this occurs when the minimum voltage appears at the other end, at the capacitor. But the capacitor sees its minimum voltage when the load step first occurs, because of its ESR. The minimum voltage on the capacitor is $V_{c,min} = V_{in} - I_{pk}$ x ESR. The voltage across the inductor is thus $V_{L,max} = V_{in} - (V_{in} - I_{pk}$ x ESR) = I_{pk} x ESR. Thus, the dI/dt of the inductor is dI/dt = I_{pk} x ESR / L, (there is no drop across the inductor's resistance because there is no current flowing yet), and this value must be less than 0.1A/µsec to meet the Intel spec.

Example: Using the 400MHz processor again, the input current is going to be 12.6A x 2.0V / 5V = 5.0A. The Sanyo capacitors selected have an ESR of 44mΩ each, for a total of 15mΩ. We need

$$L \geq \frac{I_{pk} \times ESR}{dI/dt} = \frac{5.0A \times 15m\Omega}{0.1A/\mu sec} = 0.75\mu H$$

at 5A.

It is interesting to note that the peak input current during a 12.6A load step using this value of L is less than 5.4A, according to a Spice simulation. If the inductance is tripled to 2.3µH, however, the peak current actually *increases*, because the Q of the tank is increased; the peak current is now almost 6.5A, and there is substantial ringing. Thus, the optimal value is probably one that is just equal to the value computed by the dI/dt requirements.

Notes:

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